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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/359,056	07/21/1999	BARMAK MANSOORIAN	08305/038001	2286

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Thomas J D'Amico
Dickstein Shapiro Morin & Oshinsky LLP
2101 L Streew NW
Washington, DC 20037-1526

EXAMINER

TRAN, NHAN T

ART UNIT

PAPER NUMBER

2615

DATE MAILED: 10/07/2003

14

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/359,056

Applicant(s)

MANSOORIAN, BARMAK

Examiner

Nhan T. Tran

Art Unit

2615

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 July 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 July 1999 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 – 17 have been considered but are moot in view of the new ground(s) of rejection.

Drawings

2. Figures 1 - 3(a) & (b) should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 10 is objected to because of the following informalities: the claim recites the limitation “wherein respective magnitudes of the current biases set the respective output impedances.” The limitation is not consistent with the second circuit on the image receiving circuit, wherein the input impedance is realized, not the output impedance as claimed.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1 – 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pain et al (US 5,886,659) in view of Pickering et al (US 5,050,194).

Regarding claim 1, Pain discloses an image sensor, comprising:
an image acquisition portion (100, 112) as shown in figs. 1A-1C, col. 3, lines 52-63;
an image processing portion (ADC array 118), receiving image information from said image acquisition portion, said image processing portion including a CMOS circuitry with CMOS outputs having an output impedance; said image processing portion producing a current mode output (see fig. 1C; col. 1, line 55 – col. 2, line 7; col. 5, line 65 – col. 6, line 5 & col. 7, lines 10-16). It is noted that the output impedance is inherent at the ADC array output. Since the ADC array is configured in CMOS with current driving mode, the impedance must exist in the transmission line(s) at the ADC array output.

Pain's disclosure of digital output 110 (figs. 1A-1C) suggests another separate portion (i.e., another chip) to be connected thereto for receiving digital image data output from the ADC array. The suggested separate portion represents "an image receiving portion, having an input impedance, receiving said image information from said CMOS outputs...and said image

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receiving portion receiving current mode output” in order to form a complete imaging system of CMOS compatible applications (see col. 2, lines 5-7 for a consistent CMOS compatible).

Therefore, it would have been obvious to one of ordinary skill in the art to recognize another chip connected to the digital output from the image processing portion (ADC array 118) as an image receiving portion having CMOS and input characteristics which are compatible with the digital output of the image processing portion in a complete imaging system.

Pain does not explicitly disclose that the CMOS outputs are differential outputs and an impedance matching device matches said output impedance of said image processing portion to said input impedance of said image receiving portion.

However, as taught by Pickering, differential output driver and differential input driver are implemented in CMOS technology for transmitting and receiving off-chip data, and matching impedances of the drivers with transmission line is also performed at the output and input of the drivers to minimize common mode noise and noise caused by reflections (see Fig. 1; col. 2, lines 17-26, 45-50).

Therefore, it would have been obvious to one of ordinary skill in the art to modify Pain with Pickering by implementing the CMOS differential output and input drivers with impedance matching device for transmitting and receiving off-chip data as well as minimizing common mode noise and noise caused by reflections.

Regarding claim 2, the image processing portion includes a portion with a CMOS output (3) as shown by Pickering in Fig. 1.

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Regarding claims 3 & 6, Pickering also discloses that impedance matching circuits (terminating circuits 6) are implemented at both ends (see Fig. 1; col. 2, lines 59-61).

Regarding claim 4, Pickering discloses a current source (shown in block 3 of Fig. 1) used to bias the transistors in which the corresponding impedance inherently exists at the output of each transistor in response to the bias current.

Regarding claim 5, the output impedance is matched to input impedance of the image receiving circuit as analyzed in claim 1.

Regarding claim 7, Pickering shows differential input buffer (8) at the receiver (7). It is noted that the same analysis in claim 4 is applied to claim 7 for the input impedance.

Regarding claim 8, the input impedance is matched to output impedance of the image receiving circuit as analyzed in claim 1.

Regarding claim 9, the claimed limitations are analyzed with respect to claims 3 & 6.

Regarding claim 10, the claimed limitations are analyzed with respect to claims 4 & 7.

Regarding claim 11, the claimed limitations are analyzed with respect to claims 5 & 8.

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Regarding claim 12, Pickering shows a current source used for biasing the transistors in the differential buffer 3 (Fig. 1). Pickering does not teach that the current source is a current mirror part. However, an Official Notice is taken that the current source can be configured by current mirror in CMOS applications.

Therefore, it would have been obvious to one of ordinary skill in the art to recognize that the current source in Pickering would be alternatively implemented using current mirror in a well known configuration in the art.

Regarding claim 13, Pain discloses the image acquisition circuit being an active pixel sensor (APS 300) with a photosensor (photogate 310), an in-pixel buffer (floating diffusion 330), and in-pixel select transistor (vertical select 370) (see fig. 3A; col. 6, lines 25-49).

Regarding claim 14, Pain also discloses that the image acquisition portion and the image processing portion operates at substantially zero voltage since the CMOS APS pixel and ADC array are driven in current mode, which means voltage required is very small, i.e. 0.5V for driving threshold of M1 (see col. 5, line 65 – col. 6, line 5 & col. 7, lines 10-16).

Regarding claim 15, the claimed limitations are analyzed with respect to claim 1 except for the limitations of matching impedances by adjusting bias current through at least one biased device in a way that renders the input impedance relatively independent of an input current. Pickering teaches the resistors (6) connected at both transmitter end and receiver end being used for matching impedances but Pickering does not explicitly teach that these resistors are variable.

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An Official Notice is taken that a variable resistor can be implemented using a transistor with adjustable bias current.

Therefore, it would have been obvious to one of ordinary skill in the art to modify the fixed value resistors in Pickering by providing variable resistors configured in transistors by adjusting bias currents so that a flexible impedance control between the transmitter and the receiver is realized independent of an input current.

Regarding claim 16, the claimed limitations are analyzed with respect to claims 1-15.

Regarding claim 17, the claimed limitations are analyzed with respect to claim 14.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

NT.

October 1, 2003

A handwritten signature in black ink, appearing to read 'A. Christensen', with a long horizontal flourish extending to the right.

**ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600**